

AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A device for prolonging lifetime of nonvolatile memory, the device being connected with an electronic machine and a nonvolatile memory unit, comprising a RAM (Random Access Memory) buffer zone, a counter, and two sets of inverters, wherein:

the RAM buffer zone is connected with the counter and the inverters ~~is~~ and employed for temporary storage of a unit data train and a ~~correspondent~~ corresponding state flag ~~during accessing~~ when a host electronic machine is to read/write from or to ~~a~~ the nonvolatile memory unit, wherein the state flag ~~will indicate the operation state when the unit data train passes through~~ determines whether the unit data train is to be inverted by the inverters;

the counter connected with the host electronic machine and the RAM buffer zone is in charge of counting ~~the~~ total bits of logic "0" in the unit data train and judging whether the counted result outnumbered a default proportion or not~~[[;]]~~, wherein if positive a counted result outnumbered a default proportion, the state flag corresponding to the unit data train is turned into "0", otherwise, the state flag corresponding to the unit data train is turned into "1"; and

the ~~interpolated~~ inverters are arranged to check the corresponding state flag of the unit data train ~~for inverse or non-inverse operation of~~ and invert the unit data train if the state flag has been turned into "0";

whereby the electronic machine will write ~~less~~ fewer bits of logic "0" to prolong the lifetime of the nonvolatile memory unit.

2. (Canceled)

Serial Number 09/879,979

3. (New) The device according to claim 1, wherein said default proportion is 50%, whereby whenever a number of "0"s in said data train exceeds a number of "1"s, an inverse operation is carried out on said unit data train.

4. (New) The device according to claim 1, wherein upon reading a unit data train, said inverters are arranged to again invert said unit data train, if the unit data train was previously inverted during writing as indicated by said state flag.